CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1-37. (Cancelled)

38. **(Cancelled)**

39. **(Currently Amended)** The device according to Claim ~~**38**~~ **75**, wherein

- the second unit instruction succeeds the stipulated instruction by one instruction.

40. (Previously Presented) The device according to Claim 39, wherein

- the second unit is configured to receive an increment of a count value and an identification value, which designates a thread, and
- the second unit is configured to use the increment of the count value and the identification value to determine the second unit instruction.

41. **(Currently Amended)** The device according to Claim ~~**38**~~ **75**, wherein

- the first unit is configured to activate a new context that is associated with the **first** thread ~~**assigned to the incoming data element**~~ if **[[a]] the** preceding ~~**data element is assigned to another**~~ thread **and the first thread differ**.

42. (**Currently Amended**) The device according to Claim 41, wherein

- the first unit is configured to fetch, responsive to activating the new context, a first instruction of the ~~**incoming date element**~~ **first** thread and transmit the first instruction to the third unit for decoding; and

- the first unit is configured to transmit an increment of the position that the instruction fetched by it assumes in the thread, to the second unit.

43. (Previously Presented) The device according to Claim 40, wherein

- the second unit is configured to determine the instruction that succeeds the instruction fetched by the first unit in the thread.

44. (**Currently Amended**) The device according to Claim ~~**38**~~ **75**, wherein

- the ~~**selected**~~ **first unit** instruction is repeated for successive data elements until ~~**a stipulated**~~ **the** condition is fulfilled.

45. (**Currently Amended**) The device according to Claim 44, wherein

- the third unit is configured to cause repetition of the selected instruction by causing repetition of **[[a]] the first multiplexer** control signal.

46. (**Currently Amended**) The device according to Claim ~~**48**~~ **45**, wherein

- the number of repetitions of the selected instruction is stipulated by a value;

- the third unit is configured to decrement the value in conjunction with each repetition; and

- the repetitions are interrupted when the value reaches zero.

47. (**Currently Amended**) The device according to Claim 44, wherein

- responsive to fulfillment of the ~~**stipulated**~~ condition, a stipulated instruction within a currently assigned thread is used for processing of a **next** succeeding data element ~~**entering the device next**~~ if a thread assigned to the succeeding data element is the same as the currently assigned thread.

48. (**Cancelled**)

49. (Previously Presented) The device according to Claim 47, wherein

- the stipulated instruction is the second unit instruction fetched by the second unit.

50. (**Cancelled**)

51. (**Currently Amended**) The device according to Claim 49, wherein

- the second unit instruction ~~**fetched**~~ is transmitted to the first unit and entered in a context therein.

52. (Previously Presented) The device according to Claim 47, wherein

- the stipulated instruction is fetched by the first unit and transmitted to the third unit for decoding.

53. (**Currently Amended**) The device according to Claim 47, wherein

- the third unit, after fulfillment of the ~~**stipulated**~~ condition, transmits ~~**an instruction**~~ **information** to the first unit indicative of which instruction is to be fetched.

54. (**Currently Amended**) The device according to Claim 47, wherein

- the ~~**stipulated**~~ condition comprises a condition selected from the group consisting of assertion of a signal controllable from outside of device, detection of a specific data element entering the device, detection of a specific state of the currently assigned thread, and detection of a specific instruction to be processed.

55. (Previously Presented) The device according to Claim 44, further comprising:

- a program memory including instructions for processing of the data elements and information corresponding to at least one instruction indicative of to how many data elements the instruction is to be applied.

56. (**Currently Amended**) The device according to Claim ~~**38**~~ **75**, further comprising:

- two series-connected delay units each configured to delay ~~**the**~~ **an incoming** data element by one clock cycle.

57. (**Currently Amended**) A method for controlling processing of data elements, **wherein the data elements are assigned to threads, the method** comprising:

- **storing at least one instruction of a first thread assigned to a first data element in a first set of registers of a first unit;**
- fetching by **[[a]] the** first unit a first unit instruction **from said at least one instruction of said first thread** ~~**that is stored in a context associated with the assigned thread assigned**~~;
- fetching by a second unit a second unit instruction, which succeeds a stipulated instruction in a stipulated thread, and
- **outputting, by a first multiplexer receiving said first unit instruction and said second unit instruction, a selected instruction selected from the first and second unit instructions;**
- decoding **said multiplexer output instruction** by a third unit**;** ~~**a selected instruction selected from a group consisting of the first unit instruction and the second unit instruction and generating a control signal for processing of the incoming data element**~~
- **evaluating by the third unit a condition associated with repetitive execution of the first unit instruction;**
- **comparing by the third unit a first thread associated with the first data element with a preceding thread associated with a preceding data element; and**
- **responsive to a control signal generator receiving outputs indicative of said evaluating and said comparing, generating at least one control signal including the first multiplexer control signal based, at least in part, on said outputs.**

58. (Previously Presented) The method according to Claim 57, wherein

- the second unit instruction immediately succeeds the stipulated instruction.

59. (Previously Presented) The method according to Claim 58, further comprising:

- receiving, by the second unit, an increment of a count value and an identification value, which designates a thread, and

- determining, by the second unit, the second unit instruction using the increment of the count value and the identification value

60. (**Currently Amended**) The method according to Claim 57, further comprising:

- activating, by the first unit, a context of the ~~**assigned**~~ **first** thread if a preceding data element refers to another thread.

61. (**Currently Amended**) The method according to Claim 60, further comprising:

- responsive to activating the context, by the first unit, fetching a first instruction of **[[a]] first** thread ~~**associated with the activated context**~~ as the first unit instruction and transmitting the first unit instruction to the third unit for decoding; and

- transmitting an increment of a position the first unit instruction assumes in the first thread to the second unit.

62. (Previously Presented) The method according to Claim 59, further comprising:

- determining an instruction that succeeds the instruction fetched by the first unit in the thread.

63. (Previously Presented) The method according to Claim 57, further comprising:

- decoding an instruction repetitively for successive data elements until a stipulated condition is met.

64. (**Currently Amended**) The method according to Claim 63, wherein

- repetitively decoding the instruction is accomplished by the ~~**fetching**~~ **generating** the same **first multiplexer** control signal by the third unit.

65. (Previously Presented) The method according to Claim 63, wherein

- the number of repetitions of an instruction is stipulated by a value,
- the value, during a repetition of the instruction, is decremented by the third unit, and
- the repetitions are interrupted by the value 0.

66. (Previously Presented) The method according to Claim 63, wherein

- after fulfillment of the stipulated condition a stipulated instruction within a currently assigned thread is used for a successive data element if the currently assigned thread is also assigned to the successive data element.

67. (Previously Presented) The method according to Claim 66, wherein

- an inquiry into fulfillment of the stipulated condition occurs in the third unit.

68. (Previously Presented) The method according to Claim 66, wherein

- the stipulated instruction is the second unit instruction.

69. (Previously Presented) The method according to Claim 67, wherein

- the second unit instruction is transmitted to the first unit and stored in a context of the first unit.

70. (Previously Presented) The method according to Claim 66, wherein

- the stipulated instruction is fetched by the first unit and transmitted to the third unit for decoding.

71. (Previously Presented) The method according to Claim 67, further comprising:

- after fulfillment of the stipulated condition, transmitting an instruction by the third unit to the first unit as to which instruction is to be fetched.

72. (Previously Presented) The method according to Claim 66, wherein

- the stipulated condition, whose fulfillment leads to interruption of repetitions of an instruction, is fulfilled by a signal controllable from outside of device, or by a specific data element entering the device, or by a specific state of the corresponding thread, or by a specific instruction to be processed.

73. (**Currently Amended**) A device for controlling processing of data elements **using instruction sets of the form- repeat X until Y else go to Z, where X is an instruction, Y is a condition, and Z is a target**, comprising:

- a first unit ~~**operable to store context information associated with a thread to which an incoming data element is assigned and further**~~ operable to fetch a first unit instruction ~~**wherein the first unit instruction is an instruction of the thread**~~;
- a second unit operable to fetch a second unit instruction ~~**wherein the second unit instruction**~~; and
- a third unit operable to decode instructions and further operable to ~~**generate a selection control signal wherein the selection control signal is used to select between the first unit instruction and the second unit instruction as an instruction next to be provided to and decoded by the third unit**~~ **generate at least one control signal to select the first unit instruction for decoding when the condition Y is not met and to select the second unit instruction for decoding when the condition is met and a context of an instruction at target Z is the same as a context of the instruction X**.

74. (**Currently Amended**) The device of claim 73, wherein the ~~**second unit instruction is an instruction in the thread that is a sequentially adjacent instruction succeeding the first unit instruction**~~ **third unit is further configured to select an instruction stored in a second context of the first unit for decoding when the condition is met and the context of the instruction at Z is different than the context in which the instruction X is stored**.

75. **(New)** A device for controlling processing of incoming data elements, wherein threads are assigned to the data elements, comprising:

- a first unit to fetch a first unit instruction for processing a first data element;
- a second unit to fetch a second unit instruction for processing the first data element, wherein the second unit instruction succeeds a stipulated instruction of a stipulated thread;
- a first multiplexer having a first input to receive the first unit instruction and a second input to receive the second unit instruction and a control signal input, said multiplexer being configured to produce a selected instruction selected from the first unit instruction and a second unit instruction based on the multiplexer control signal; and
- a third unit configured to receive the selected instruction, comprising:
  - a decoder to decode the selected instruction;
  - a condition evaluator to evaluate a condition associated with repetitive execution of the first unit instruction;
  - a thread comparator to compare a first thread associated with the first data element with a preceding thread associated with a preceding data element; and
  - a control signal generator receiving outputs from said condition evaluator and said thread comparator and configured to generate at least one control signal including the first multiplexer control signal based, at least in part, on said outputs.